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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/728,022	WILLIAMS ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 7-13 and 17-20 remain pending in the current application.

Response to Arguments

2. Applicant's arguments, see Appeal Brief filed 12/08/06, with respect to claim 7 have been considered but are moot in view of the new ground(s) of rejection. Applicant's arguments concerning claim 17 have been fully considered but they are not persuasive.

As per the arguments per claim 7:

The Applicants argues on pages 12-13, "Appellants respectfully submit that Jarwala fails to disclose or suggest the recited IC tester and IC DUT", "the random number generator and the selector circuit are included on the integrated circuit device under test (IC DUT). In contrast, Jarwala teaches testing a circuit board 12, wherein each circuit board 12 includes a plurality of electrical components 15, such as ICs. Therefore, Jarwala fails to teach the recited IC DUT" and "the first and second memories are included on an IC tester. The Examiner ignores this limitation". The Examiner will address these arguments in the newly submitted rejection below.

The Applicants' go on to state "Jarwala cannot achieve the tester throughput and the performance provided by Applicants' recited testing system". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *tester throughput*

and the performance provided by Applicants' recited testing system) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As per the arguments per claim 17:

The Applicants argues on page 14, "Jarwala fails to disclose or suggest the recited step of supplying the output generated by the circuit block to an input of a stage of the random number generator (i.e. step g))". The Examiner respectfully disagrees and asserts the Jarwala substantially teaches the above stated limitations. Jarwala teaches the Automatic Test Pattern Generator (ATPG) 34 typically takes the form of a Linear Feedback Shift Register (LFSR) (**a random number generator**) that generates a separate one of four different patterns of test vectors in accordance with information stored in the Test Vector Manipulation register (**supplying said output generated by said circuit block to an input of a stage of said LFSR**) within the BSM internal register bank 29. Jarwala teaches the responses generated by the circuit board 12.sub.1 of FIG. 1 (circuit block) are also compacted by a Linear Feedback Shift Register 40. (Col. 5, ll. 39-45). The Applicants' go on to state "The recited step, as discussed in reference to FIG. 4B, can interleave output values from the DUT into the LFSR, thereby advantageously increasing the effective randomness of the result as well as error detection capability". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., increasing the *effective randomness of the result as well as*

error detection) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is the Examiner's conclusion that independent claim 17 is not patentably distinct or non-obvious over the prior arts of record namely, Jarwala et al. (US-5444716). Therefore, the rejection is maintained. Based on their dependency on independent claim 7, claims 18-20, stand rejected.

Claim Objections

3. In the interest of maintaining conformity with the instantiation of an antecedent in each of the independent claims, the examiner objects to dependent Claims 8-13 and 18-20 because the claims do not refer back to the independent claim, but rather give the impression that there is a new method/module/system being claimed. In other words, the examiner requests that the applicant change the first word of each of the above dependent claims from "An" or "A" to "The".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-10, 13, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala et al. (US-5444716), hereinafter Jarwala.

Claims 7-9:

Jarwala teaches a register bank 29 that is coupled via a bidirectional bus 30 to a first memory bank (32) (**second memory**) and to an automatic test pattern generator 34 (**a random number generator**). Jarwala teaches the first memory bank 32 is designated as a Test Vector Output (TVO) memory (**second memory**) because it stores a set of deterministic test vectors for testing the circuit board 12.sub.1 of FIG. 1. Jarwala also teaches the vectors in the TVO memory 32 are generated in advance of testing. Jarwala further teaches the Automatic Test Pattern Generator (ATPG) 34 typically takes the form of a Linear Feedback Shift Register (LFSR per claim 9) (**a random number generator**) that generates a separate one of four different patterns of test vectors in accordance with information stored in the Test Vector Manipulation register (**based on a seed**) within the BSM internal register bank 29. Jarwala even further teaches the TVO memory 32 (**second memory**) and the APTG 34 (**a random number generator**) are coupled to a first and a second input, respectively, of a multiplexer 36 (**selector circuit**) that passes the signal at a selected one of its first and second inputs to its output, designated as the Test Data Output (TDO) of the BSM 20.sub.1 (**coupling to said integrated circuit**) which is coupled to a test data input of the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1. (Col. 5, ll. 14-33, Fig. 2). Jarwala does not explicitly disclose "**a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a**

plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random". However, Jarwala does disclose a Test Vector Manipulation Register (**first memory**) that provides the primary test resource control for determining the source of test vectors supplied to the circuit board. Jarwala also discloses this register also determines the destination for responses generated during testing. (Col. 4, ll. 34-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Jarwala's Test Vector Manipulation Register suggests a first memory for storing a mask vector for characterizing corresponding test vector data. The artisan would have been motivated to conclude this because the Test Vector Manipulation Register comprises of memory elements for storing test resource control (**mask vector**) for determining the source of test vectors supplied to the circuit board (for switching between TVO memory 32 (**deterministic test vector data**) and the APTG 34 (**pseudo random test vector data**)).

Jarwala does not explicitly teach the random number generator and selector circuit are located in the DUT. However, Jarwala does teach automatic test pattern generator 34 (**a random number generator**) and multiplexer 36 (**selector circuit**) are located within the BSM. It would have been obvious to one of ordinary skill in the art at the time the invention was made to relocate the automatic test pattern generator 34 and multiplexer 36 into the DUT (one of the electronic components 14_1-14_p, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In*

re Japikse, 86 USPQ 70 (CPA 1950). Applicants' Figures 2 and 3 further illustrate this obviousness of rearranging parts, where LFSR 230 and selector 225 are moved into DUT 16 to form new DUT 16' in Fig. 3.

Claims 17:

Jarwala teaches a register bank 29 that is coupled via a bidirectional bus 30 to a first memory bank (32) (**second memory**) and to an automatic test pattern generator 34 (**a random number generator**). Jarwala teaches the first memory bank 32 is designated as a Test Vector Output (TVO) memory (**second memory**) because it stores a set of deterministic test vectors for testing the circuit board 12.sub.1 of FIG. 1. Jarwala also teaches the vectors in the TVO memory 32 are generated in advance of testing. Jarwala further teaches the Automatic Test Pattern Generator (ATPG) 34 typically takes the form of a Linear Feedback Shift Register (LFSR per claim 9) (**a random number generator**) that generates a separate one of four different patterns of test vectors in accordance with information stored in the Test Vector Manipulation register (**based on a seed**) within the BSM internal register bank 29. Jarwala even further teaches the TVO memory 32 (**second memory**) and the APTG 34 (**a random number generator**) are coupled to a first and a second input, respectively, of a multiplexer 36 (**selector circuit**) that passes the signal at a selected one of its first and second inputs to its output, designated as the Test Data Output (TDO) of the BSM 20.sub.1 (**coupling to said integrated circuit**) which is coupled to a test data input of the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1. (Col. 5, ll. 14-33, Fig. 2).

"e) applying said output test vector to said circuit block;"

Jarwala teaches the TDO output of the BSM 20.sub.1 is coupled to a test data input of the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1. (Col. 5, ll. 31-33).

"f) obtaining an output generated by said circuit block in response to said output test vector;"

Jarwala teaches the TVI memory bank 38 stores responses generated by the chain of Boundary-Scan cells 14.sub.1 -14.sub.p of FIG. 1, in response to test vectors supplied thereto, via the multiplexer 36. (Col. 5, ll. 36-38).

"g) supplying said output generated by said circuit block to an input of a stage of said LFSR."

Jarwala teaches the Automatic Test Pattern Generator (ATPG) 34 typically takes the form of a Linear Feedback Shift Register (LFSR) (**a random number generator**) that generates a separate one of four different patterns of test vectors in accordance with information stored in the Test Vector Manipulation register (**supplying said output generated by said circuit block to an input of a stage of said LFSR**) within the BSM internal register bank 29. Jarwala teaches the responses generated by the circuit board 12.sub.1 of FIG. 1 (circuit block) are also compacted by a Linear Feedback Shift Register 40. (Col. 5, ll. 39-45).

Jarwala does not explicitly disclose "**retrieving a mask vector from a first memory, said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a**

second bit value indicates that said corresponding test vector data is pseudo random". However, Jarwala does disclose a Test Vector Manipulation Register (**first memory**) that provides the primary test resource control for determining the source of test vectors supplied to the circuit board. Jarwala also discloses this register also determines the destination for responses generated during testing. (Col. 4, ll. 34-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Jarwala's Test Vector Manipulation Register suggests a first memory for storing a mask vector for characterizing corresponding test vector data. The artisan would have been motivated to conclude this because the Test Vector Manipulation Register comprises of memory elements for storing test resource control (**mask vector**) for determining the source of test vectors supplied to the circuit board (for switching between TVO memory 32 (**deterministic test vector data**) and the APTG 34 (**pseudo random test vector data**)).

Claim 10:

"an output of said circuit block is coupled to an input of one stage of said LFSR."

Jarwala teaches the responses generated by the circuit board 12.sub.1 of FIG. 1 (circuit block) are also compacted by a Linear Feedback Shift Register 40. (Col. 5, ll. 39-45).

Claim 13 and 19:

Jarwala teaches the vectors in the TVO memory 32 are generated in advance of testing. (Col. 5, lines 19, 20). It would have been obvious to one of ordinary skill in the

art at the time the invention was made that the vectors generated in advance (deterministic test vector data) that are stored in the TVO memory 32 (second memory) would be generated by an automatic test pattern generator (ATPG) process. The artisan would have been motivated to do so because automatic test pattern generator (ATPG) processes are used for generating deterministic test vector data.

Claim 20:

Jarwala teaches the Boundary-Scan cells 14_1 -14_p each comprise a single-bit register associated with a node of an electronic component 15, such as an integrated circuit or the like. (Col. 3, ll. 8-11).

5. Claims 11, 12, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala et al. (US-5444716), hereinafter Jarwala in view of Lesmeister (US-6101622), hereinafter Lesmeister.

Claims 11, 12 and 18:

Jarwala does not explicitly disclose "said mask vector is data compressed" and "a decompressor coupled between said first memory and said selector circuit". However, Jarwala does disclose a Test Vector Manipulation Register (first memory) that provides the primary test resource control for determining the source of test vectors supplied to the circuit board. Lesmeister teaches each DATA value stored in FIFO buffer 28 (first memory) is a compressed version of a set of one or more vectors. Lesmeister also teaches decompressor circuit 30 decompresses each read out DATA word to produce a sequence of one or more vectors which includes an input "mode

selection" field (MODE_SEL). (Col. 4, ll. 57, 58, 62, 63, col. 5, ll. 42-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jarwala's Test Vector Manipulation Register (first memory) to include Lesmeister's FIFO buffer 28 (first memory). The artisan would have been motivated to do so because it would enable Jarwala to store compressed data as a mask vector and to save storage capacity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jarwala's internal register bank 29 to incorporate Lesmeister's decompressor circuit 30. The artisan would have been motivated to do so because it would enable Jarwala to decompress Lesmeister's "mode selection" field (MODE_SEL) from the first memory and provide the decompressed mode select to the selector circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 3/13/07
Examiner
Art Unit 2138